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09/715,778	11/17/2000	Jack B. Dennis	004800.P003	7027

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EXAMINER	
MEW, KEVIN D	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 09/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/715,778	DENNIS, JACK B.	
	Examiner	Art Unit	
	Kevin Mew	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/17/2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 1-30** are rejected under 35 U.S.C. 102(e) as being anticipated by Blelloch et al. (USP 6,434,590).

Regarding claims 1, 11, Blelloch discloses an apparatus to perform a method comprising:

a priority register (priority queue) to store thread information for P threads (priority queue in which each element of the queue is a thread. In particular, the threads are P threads, see col. 14, lines 60-67, col. 15, lines 1-15, and col. 16, lines 16-21), the thread information including P priority codes corresponding to the P threads (the thread information indicates whether the threads are ready, active, or suspended, see col. 14, lines 65-67), at least one of the P-threads requesting use of at least one resource unit (task queue uses the program and feedback information obtained from processing elements PE1 to update the task queue, see col. 3, lines 60-64) ; and

a priority selector (assignment manager) coupled to the priority register (assignment manager is coupled to task queue, see AM1 and TQ1, Fig. 4) to generate assignment signal to assign (assignment manager informs the processing elements PE1 about the availability of tasks, see col. 4, lines 38-59) the at least one resource unit (processing elements PE1, see col. 4, line

48) to the at least one of the P threads (highest priority available task) according to the P priority codes (makes the highest priority available tasks to be drawn by the processing elements PE1, see col. 4, lines 44-48, see Figs. 1, 2, 4).

Regarding claims 2, 12, Blelloch discloses the apparatus of claim 1 to perform the method of claim 11 wherein the at least one resource unit is one of an instruction unit, an instruction buffer, a memory locking unit, a load unit, a store unit, an input/output unit, a peripheral unit interface, and a functional unit (the resource unit is processing elements PE1, which are functional units, see col. 3, lines 52-64, see Figs 1, 2, 4).

Regarding claims 3, 13, Blelloch discloses the apparatus of claim 2 to perform the method of claim 12 wherein the functional unit is one of an arithmetic unit, a logic unit, and an arithmetic and logic unit (processing elements PE1 comprises computational elements CE1, see col. 3, lines 9-19 and Fig. 2a).

Regarding claims 4, 14, Blelloch discloses the apparatus of claim 1 to perform the method of claim 11 further comprising:

an instruction multiplexer (see system SY1 of processing elements, Fig. 2) coupled to the priority selector (assignment manager, see Fig. 1) to pass instructions stored in a plurality of instruction registers (SY1 comprises a plurality of memory elements ME of the processing elements PE1, see col. 3, lines 9-19, and Fig. 2a) to execution units according to the assignment signal (to the computational units CE of the processing elements, see Fig. 2a).

Regarding claims 5, 15, Blelloch discloses the apparatus of claim 1 to perform the method of claim 11 further comprising:

a priority assignor (a sequential scheduler, see col. 4, lines col. 4, 22-37) coupled to the priority register to set the thread information including at least one of the P priority codes corresponding to the at least one of the P threads (a sequential scheduler designates each task with a code that identifies the ordering of the task in the sequence of instructions, see col. 4, lines 9-14) in response to a start instruction from an instruction decoder and dispatcher (preprocessor PP1, see steps 507, 508, Fig. 5).

Regarding claims 6, 16, Blelloch discloses the apparatus of claim 5 to perform the method of claim 15 wherein the priority assignor sets an active flag in the priority register corresponding to the at least one of the P threads in response to the start instruction (a sequential scheduler sets available flag for those tasks that are available for scheduling, see col. 4, lines 22-37).

Regarding claims 7, 17, Blelloch discloses the apparatus of claim 6 to perform the method of claim 16 wherein resets the active flag in the priority register corresponding to the at least one of the P threads in response to a quit instruction from the instruction decoder and dispatcher (resets the live flag for a thread when the end instruction executes, see col. 11, lines 29-35).

Regarding claims 8, 18, Blelloch discloses the apparatus of claim 1 to perform the method of claim 11 wherein the priority selector assigns the at least one resource unit to the at least one of the P threads if the at least one of the P threads is not served (assignment manager determines which the set of tasks that are live, see step 510, Fig. 5) and the at least one resource unit is free (each processing element draws tasks from the assignment manager (see col. 2, lines 52-67).

Regarding claims 9, 19, Blelloch discloses the apparatus of claim 8 to perform the method of claim 18 wherein the at least one of the P threads has highest priority code among a set of ready threads of the P threads (see col. 4, lines 38-48).

Regarding claims 10, 20, Blelloch discloses the apparatus of claim 8 to perform the method of claim 18 wherein the priority selector iteratively assigns resource units to threads in the set of ready threads of the P threads according to the corresponding priority codes and resource availability until the set becomes empty (see col. 20, lines 34-38).

Regarding claim 21, Blelloch discloses a processor (a processor here is a combination of preproceesor, assignment manager and system of processing elements, see Fig. 1) comprising:

at least one a resource unit (system of processing elements PE, see Figs. 2 and 2a) to provide resource for use by P threads (provides program and feedback information to the task queue, see col. 3, lines 60-64); and

a resource prioritizer (a resource prioritizer here is a combination of preprocessor and assignment manager, see Fig. 1) coupled to the resource unit (system of processing elements PE, see Figs. 2 and 2a) to prioritize resource utilization (for determining priorities among tasks, see col. 4, lines 16-59), the resource prioritizer comprising:

a priority register (priority queue) to store thread information for P threads (priority queue in which each element of the queue is a thread. In particular, the threads are P threads, see col. 14, lines 60-67, col. 15, lines 1-15, and col. 16, lines 16-21), the thread information including P priority codes corresponding to the P threads (the thread information indicates whether the threads are ready, active, or suspended, see col. 14, lines 65-67), at least one of the P-threads requesting use of at least one resource unit (task queue uses the program and feedback information obtained from processing elements PE1 to update the task queue, see col. 3, lines 60-64) ; and

a priority selector (assignment manager) coupled to the priority register (assignment manager is coupled to task queue, see AM1 and TQ1, Fig. 4) to generate assignment signal to assign (assignment manager informs the processing elements PE1 about the availability of tasks, see col. 4, lines 38-59) the at least one resource unit (processing elements PE1, see col. 4, line 48) to the at least one of the P threads (highest priority available task) according to the P priority codes (makes the highest priority available tasks to be drawn by the processing elements PE1, see col. 4, lines 44-48, see Figs. 1, 2, 4).

Regarding claim 22, Blelloch discloses the processor of claim 21 wherein the at least one resource unit is one of an instruction unit, an instruction buffer, a memory locking unit, a load

unit, a store unit, an input/output unit, a peripheral unit interface, and a functional unit (the resource unit is processing elements PE1, which are functional units, see col. 3, lines 52-64, see Figs 1, 2, 4).

Regarding claim 23, Blelloch discloses the processor of claim 22 wherein the functional unit is one of an arithmetic unit, a logic unit, and an arithmetic and logic unit (processing elements PE1 comprises computational elements CE1, see col. 3, lines 9-19 and Fig. 2a).

Regarding claim 24, Blelloch discloses the processor of claim 21 the resource prioritizer further comprising:

an instruction multiplexer (see system SY1 of processing elements, Fig. 2) coupled to the priority selector (assignment manager, see Fig. 1) to pass instructions stored in a plurality of instruction registers (SY1 comprises a plurality of memory elements ME of the processing elements PE1, see col. 3, lines 9-19, and Fig. 2a) to execution units according to the assignment signal (to the computational units CE of the processing elements, see Fig. 2a).

Regarding claim 25, Blelloch discloses the processor of claim 21 wherein the resource prioritizer further comprising:

a priority assignor (a sequential scheduler, see col. 4, lines col. 4, 22-37) coupled to the priority register to set the thread information including at least one of the P priority codes corresponding to the at least one of the P threads (a sequential scheduler designates each task with a code that identifies the ordering of the task in the sequence of instructions, see col. 4, lines

9-14) in response to a start instruction from an instruction decoder and dispatcher (preprocessor PP1, see steps 507, 508, Fig. 5).

Regarding claim 26, Blelloch discloses the processor of claim 25 wherein the priority assignor sets an active flag in the priority register corresponding to the at least one of the P threads in response to the start instruction (a sequential scheduler sets available flag for those tasks that are available for scheduling, see col. 4, lines 22-37).

Regarding claim 27, Blelloch discloses the processor of claim 26 wherein resets the active flag in the priority register corresponding to the at least one of the P threads in response to a quit instruction from the instruction decoder and dispatcher (resets the live flag for a thread when the end instruction executes, see col. 11, lines 29-35).

Regarding claim 28, Blelloch discloses the processor of claim 21 wherein the priority selector assigns the at least one resource unit to the at least one of the P threads if the at least one of the P threads is not served (assignment manager determines which the set of tasks that are live, see step 510, Fig. 5) and the at least one resource unit is free (each processing element draws tasks from the assignment manager (see col. 2, lines 52-67).

Regarding claim 29, Blelloch discloses the processor of claim 28 wherein the at least one of the P threads has highest priority code among a set of ready threads of the P threads (see col. 4, lines 38-48).

Regarding claim 30, Blelloch discloses the processor of claim 28 wherein the priority selector iteratively assigns resource units to threads in the set of ready threads of the P threads according to the corresponding priority codes and resource availability until the set becomes empty (see col. 20, lines 34-38).

Conclusion

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure with respect to prioritizing resource utilization in multi-thread computing system.

US Patent 5,349,656 to Kaneko et al.

US Patent 5,325,526 to Cameron et al.

US Patent 5,155,858 to DeBruler et al.

US Patent 6,038,604 to Bender et al.

US Patent 6,070,189 to Bender et al.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Mew whose telephone number is 703-305-5300. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 703-305-4366. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KDM
Art Unit 2664